IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Koichi Yoshihara
Serial No.:	10/613,577
Filed:	July 2, 2003
For:	HALF-SYMBOL CONSTELLATION DISPLAY
Examiner:	Ted M. Wang
Art Unit:	2611
Confirmation No.:	4481

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Appeal Brief in Accordance With 37 C.F.R. § 41.37

Dear Sir:

This is an appeal from the Examiner's Final Rejection of the above-identified application dated July 29, 2009.

No additional fee is believed due. However, if an additional fee is due please charge that fee to Deposit Account 20-0352.

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Real Party in Interest

The real party in interest in this case is Appellant's assignee, Tektronix, Inc., an Oregon corporation, which is a subsidiary of Danaher Corporation, a Delaware corporation.

Related Appeals and Interferences

There are no prior and pending appeals, interferences, or judicial proceedings known to Appellant, Appellant's legal representative, or assignee which may be related to, directly affect, or have a bearing on the Board's decision in this appeal.

Status of Claims

Claims 2-7 have been allowed.

Claims 9 and 10 stand rejected under 35 U.S.C. § 103(a) and are being appealed.

Claims 11-14 are objected to.

Claims 1 and 8 have been cancelled.

Status of Amendments

No amendments have been submitted by Appellant after the Examiner's Final Rejection.

Summary of Claimed Subject Matter

Independent claim 2 is an apparatus for displaying a modulated signal representing symbols of information to observe distortions comprising:

means for deriving quadrature component signals (See Figure 15 and page 11, lines 1-13: antenna **10**, down converter **12**, bandpass filter **14**, demodulators **16** and **22**, carrier recovery circuit **18**, 90° phase shifter **20**, and lowpass filters **24** and **26**, wherein the quadrature component signals are the outputs of lowpass filters **24** and **26**) and a symbol clock (See Figure 15 and page 11, lines 13-14: symbol timing recovery circuit **28**) from the modulated signal (See Figure 15: received at antenna **10**);

means for generating a sample clock having a period equal to the symbol clock, the sample clock being shifted one-half period in phase with respect to the symbol clock (See Figure 15 and page 11, lines 17-18: delay module **30**);

means for sampling the quadrature component signals with the sample clock (See Figure 15 and page 11, line 18: A/D converters **32** and **34**) to produce pseudo-symbols as pairs of pseudo-symbols about a symbol sample point for each symbol ("Pseudo-symbols" are discussed in detail at page 7, line 22 – page 8, line 5.); and

means for displaying the pseudo-symbols on a quadrature coordinate plane (See Figure 15 and page 11, line 23: display **38**).

Independent claim 9 is a method of displaying pseudo-symbols on a receiver comprising the steps of:

receiving a modulated signal representing symbols of information (See Figure 15: received at antenna **10**);

deriving quadrature component signals from the modulated signal (See Figure 15 and page 11, lines 1-13: antenna **10**, down converter **12**, bandpass filter **14**, demodulators **16** and **22**, carrier recovery circuit **18**, 90° phase shifter **20**, and lowpass filters **24** and **26**, wherein the quadrature component signals are the outputs of lowpass filters **24** and **26**);

generating a sample clock having a period equal to the period of a symbol clock for the modulated signal, the sample clock being shifted one-half period in phase with respect to the symbol clock (See Figure 15 and page 11, lines 13-14: symbol timing recovery circuit **28**);

sampling the quadrature component signals using the sample clock (See Figure 15 and page 11, line 18: A/D converters **32** and **34**) to produce pseudo-symbols as pairs of pseudo-symbols about a symbol sample point for each symbol ("Pseudo-symbols" are discussed in detail at page 7, line 22 – page 8, line 5.); and

displaying the pseudo-symbols on a quadrature coordinate plane (See Figure 15 and page 11, line 23: display **38**).

Grounds of Rejection to be Reviewed on Appeal

Whether claims 9 and 10 are unpatentable under 35 U.S.C. § 103(a).

Argument

In the Final Rejection dated July 29, 2009, the Examiner rejected claims 2 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,920,220) ("Takao") in view of the admitted prior art of the present application ("the APA"); rejected claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Takao in view of the APA and further in view of Touzni et al. (U.S. Patent No. 7,031,405) ("Touzni"); objected to claims 4-7 and 11-14 as being dependent upon a rejected base claim, but indicated that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In the Advisory Action dated August 27, 2009, the Examiner maintained the rejection against claims 9 and 10, but indicated that claims 2 and 3 were allowed without explanation, as well as claims 4-7 which depend from them.

Appellant is confused as to why the Examiner would maintain the rejection against claims 9 and 10 while allowing claims 2 and 3, because claims 9 and 10 are essentially equivalent to claims 2 and 3 but in a different form (claims 9 and 10 are in method form whereas claims 2 and 3 are in means-plus-function form), and in the Final Rejection the Examiner had only rejected these claims under 35 U.S.C. § 103(a), which is not a subject-matter-based rejection. For this reason and other reasons discussed below, Appellant is not entirely certain what the Status of the Claims is. Erring on the side of caution, Appellant will present arguments below in response to every rejection given in the Final Rejection.

Appellant asserts that claims 2, 3, 9, and 10 are not rendered obvious by the cited prior art, and that the Examiner has not established a *prima facie* case of obviousness because the

Examiner has failed to properly ascertain the scope and content of the cited prior art. *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007).

Rejection of Claims 2, 3, 9, and 10 under 35 U.S.C. § 103(a)

Before addressing the substance of the rejection, Appellant wishes to address the following statement by the Examiner:

> [Claim 2] recites "means for deriving quadrature component signals and a symbol clock from the modulated signal; means for generating a sample clock having . . ." The Examiner interprets this limitation as "deriving quadrature component signals and a symbol clock from the modulated signal; generating a sample clock having . . ." since there is no Disclosure or Insufficient Disclosure of the Structure, Material, or Acts for Performing the Function Recited in a Claim Limitation Invoking 35 U.S.C. 112, Sixth Paragraph. However, the written description fails to disclose the corresponding structure, material, or acts for the claimed function. (Final Rejection, page 3, emphasis in original)

Appellant is puzzled by the Examiner's statement for two reasons:

First, Appellant is puzzled by the Examiner's assertion that the written disclosure fails to disclose the structure, material, or acts for performing the claimed function because the specification is replete with structure, material, or acts. For example, at page 11, lines 1-18 and Figure 15, it is readily apparent that the "means for deriving quadrature component signals and a symbol clock from the modulated signal" is performed by antenna 10, down converter 12, bandpass filter 14, demodulators 16 and 22, carrier recovery circuit 18, 90° phase shifter 20, lowpass filters 24 and 26, and symbol timing recovery circuit 28, and the "means for generating a sample clock having . . ." is performed by delay module 30.

Second, Appellant is puzzled by the fact that the Examiner interprets the limitations of Appellant's claim 2 which is in means-plus-function form to be *steps of a method claim*. Even if, as the Examiner asserts, the written description did not disclose the structure, material, or acts for performing the claimed function, interpreting a means claim to be a method claim is entirely

improper because there is no legal basis for such an interpretation. If a means claim is not supported by sufficient disclosure, then as MPEP § 2181 explains, the proper course of action is a rejection under 35 U.S.C. § 112 ¶ 1 and/or ¶ 2. Appellant requested that the Examiner cite legal authority to support this position, however the Examiner declined to provide any.

Now, turning to the substance of the rejection:

Independent claims 2 and 9 are not rendered obvious by Takao and the APA because neither Takao nor the APA nor their combination describes the means for or the step of "deriving . . . a symbol clock . . . ," or alternatively, "sampling the quadrature component signals . . . ," for the reasons discussed below.

The Examiner asserts that Takao's Figure 35 describes every element of claim 2 except "means for displaying the pseudo-symbols on a quadrature coordinate plane." For the convenience of the Board, a copy of Takao's Figure 35 is provided below, including the locations of Appellant's claim limitations as alleged by the Examiner:

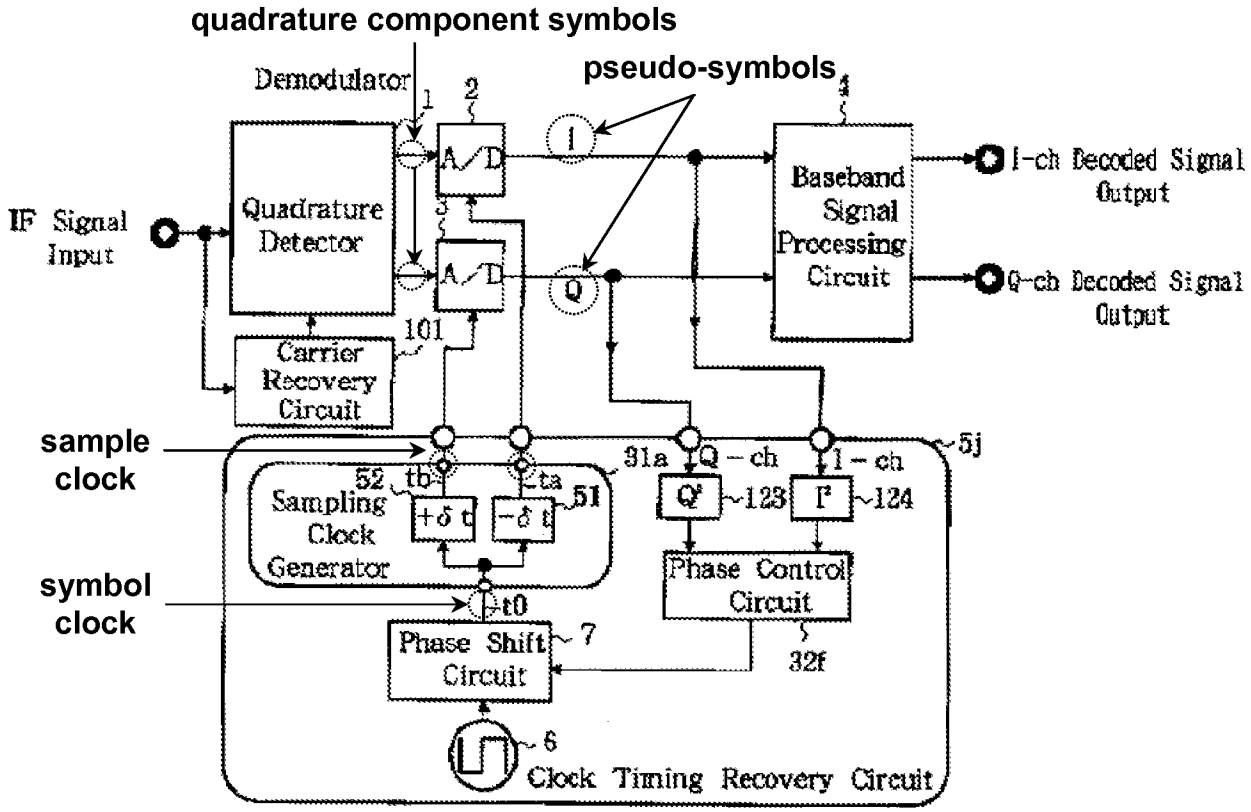

FIG.35

Now, in detail, the Examiner asserts the following:

1) Appellant's "means for deriving quadrature component signals and a symbol clock from the modulated signal" is described by Takao's Clock Timing Recovery Circuit 5j, where the Examiner considers the two outputs of Takao's quadrature detector 1 to be equivalent to Appellant's "quadrature component signals," and considers Takao's signal t0 to be equivalent to Appellant's "symbol clock." Appellant notes that on page 3 of the Final Rejection, the Examiner writes that he considers Appellant's "modulated signal" to be described by Takao's "IF Signal" (". . . is derived from the IF input signal (modulated signal)"), however on page 4 the Examiner writes that he considers Appellant's "modulated signal" to be described by Takao's "I and Q signals" (". . . based on the input modulated signal I and Q"). In the discussion below, Appellant will assume that the Examiner considers Takao's "IF Signal" to be equivalent to Appellant's "modulated signal" because it is consistent with the Examiner's position that the two outputs of

Takao's quadrature detector 1 are equivalent to Appellant's "quadrature component signals." Appellant further notes that since it is Takao's quadrature detector 1 that converts the alleged "modulated signal" into the alleged "quadrature component signals," it follows that the Examiner must also have meant to assert that Takao's quadrature detector 1 is the "means for deriving quadrature component signals." Importantly, Appellant further notes that since Takao's A/D converters 2 and 3 sample the alleged "quadrature component signals" to provide the I and Q signals as inputs to the Clock Timing Recovery Circuit 5j, it follows that the Examiner must also have meant to assert that Takao's A/D converters 2 and 3 are part of the "means for deriving . . . a symbol clock."

2) Appellant's "means for generating a sample clock having a period equal to the symbol clock, the sample clock being shifted one-half period in phase with respect to the symbol clock" is described by Takao's phase delay circuits 51 and 52, where the Examiner considers the outputs of the phase delay circuits 51 and 52 to be equivalent to Appellant's "sample clock."

3) Appellant's "means for sampling the quadrature component signals with the sample clock to produce pseudo-symbols as pairs of pseudo-symbols about a symbol sample point for each symbol" is described by Takao's A/D converters 2 and 3, where the Examiner considers the outputs of the A/D converters, i.e., the I and Q signals, to be equivalent to Appellant's "pseudo-symbols."

Appellant respectfully asserts that the Examiner's interpretation of Takao is improper because the Examiner uses Takao's A/D converters 2 and 3 to describe both Appellant's "means for deriving . . . a symbol clock . . . " and "means for sampling the quadrature component signals . . ." (underlined above). However, Takao's A/D converters 2 and 3 cannot be used to satisfy both claim limitations.

In response, the Examiner writes:

> The claim limitation does not limit "**deriving a symbol clock** and **generating a symbol clock**" to be two different circuits without overlapping or feedback. (Final Rejection, page 3, emphasis in original)

Appellant respectfully disagrees. During patent examination, pending claims must be "given their broadest reasonable interpretation . . ." See MPEP § 2111, citing *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (emphasis added). The Examiner's interpretation of claims 2 and 9 is unreasonable because it is contrary to the well-known canon of claim construction that a claim should not to be construed so as to render a claim limitation to be superfluous or redundant. See § 4.03[E][4] of "Patent Claim Construction," Robert C. Kahrl, Aspen Publishers, 2009 Supplement, and in particular the discussion regarding *Elekta Instrument S.A. v. O.U.R. Scientific International, Inc.*, 214 F.3d 1302 (Fed. Cir. 2000) (rejecting a claim construction that renders a claim limitation to be "superfluous") and *Unique Concepts, Inc. v. Brown*, 939 F.2d 1558 (Fed. Cir. 1991) (rejecting a claim construction that renders a claim limitation to be "redundant"). Specifically, in applying claims 2 and 9 to Takao, the Examiner construes the claim limitation "means for sampling the quadrature component signals with the sample clock to produce pseudo-symbols . . . " to be superfluous and redundant as follows: First, the Examiner asserts that Takao describes "means for deriving . . . a symbol clock from the modulated signal" where Takao generates the signal t0 from the IF input signal "via elements 1, 2, 3, 123, 124, 32f, and 7." (Final Rejection, page 3) Note that during the process of generating t0 from the IF input signal, A/D converters 2 and 3 must sample the output signals of the quadrature detector 1 to generate the I and Q signals. Then, the Examiner asserts that Takao describes "means for sampling the quadrature component signals with the sample clock to produce pseudo-symbols . . . " where A/D converters 2 and 3 sample the outputs of the

quadrature detector 1 to generate the I and Q signals. However, recall that the A/D converters 2 and 3 *already* sampled the output signals of the quadrature detector 1 in order to generate the I and Q signals in the "means for deriving . . . a symbol clock from the modulated signal." Thus, the Examiner's construction of claims 2 and 9 unreasonably renders the claim limitation "means for sampling the quadrature component signals with the sample clock to produce pseudo-symbols . . . " to be superfluous and redundant.

Nothing in the APA remedies this deficiency in the Examiner's interpretation of Takao.

For all of these reasons, claims 2 and 9 are not rendered obvious by Takao and the APA. Accordingly, Appellant requests that the rejection of claims 2 and 9 under 35 U.S.C. § 103(a) be reversed.

Rejection of Claims 3 and 10 under 35 U.S.C. § 103(a)

The Examiner rejected claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Takao in view of the APA and further in view of Touzni.

Claims 3 and 10 are allowable because they depend from claims 2 and 9 respectively, both of which are allowable for the reasons discussed above. Furthermore, the addition of Touzni does not remedy any of the deficiencies of the Examiner's proposed combination regarding claims 2 and 9 discussed above.

For these reasons, claims 3 and 10 are not rendered obvious by Takao in view of the APA and further in view of Touzni. Accordingly, Appellant requests that the rejection of claims 3 and 10 under 35 U.S.C. § 103(a) be reversed.

Objection to Claims 4-7 and 11-14

The Examiner objected to claims 4-7 and 11-14 as being dependent upon a rejected base claim, but indicated that they would be allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims.

Claims 4-7 and 11-14 are allowable in their present form because they depend from claims 2 and 9 respectively, both of which are allowable for the reasons discussed above. Accordingly, Appellant requests that the objection to claims 4-7 and 11-14 be reversed.

Conclusion

For all these reasons, Appellant requests that the Examiner's rejection of claims 2, 3, 9, and 10 be reversed, and that this case be passed on to issuance.

Respectfully submitted,

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December 10, 2009

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Claims Appendix

1. (Cancelled)

2. (Previously Presented) An apparatus for displaying a modulated signal representing symbols of information to observe distortions comprising:

means for deriving quadrature component signals and a symbol clock from the modulated signal;

means for generating a sample clock having a period equal to the symbol clock, the sample clock being shifted one-half period in phase with respect to the symbol clock;

means for sampling the quadrature component signals with the sample clock to produce pseudo-symbols as pairs of pseudo-symbols about a symbol sample point for each symbol; and

means for displaying the pseudo-symbols on a quadrature coordinate plane.

3. (Previously Presented) The apparatus as recited in claim 2 further comprising means for generating a template for the displaying means representing an ideal modulated signal.

4. (Original) The apparatus as recited in claim 3 further comprising means for determining a distortion index as a function of the number of pseudo-symbols that are outside the template.

5. (Original) The apparatus as recited in claim 3 wherein the template comprises a plurality of circles representing clusters of the pseudo-symbols for each symbol of the ideal modulated signal.

6. (Original) The apparatus as recited in claim 5 wherein each circle comprises a cluster outline having a diameter that is a function of an outer pair of pseudo-symbols for the corresponding symbol of the ideal modulated signal.

7. (Previously Presented) The apparatus as recited in claim 2 wherein the displaying means comprises means for zooming in on individual clusters of pseudo-symbols to observe whether the arrangement of pseudo-symbols in the cluster is similar to the arrangement of clusters on the quadrature coordinate plane.

8. (Cancelled)

9. (Previously Presented) A method of displaying pseudo-symbols on a receiver comprising the steps of:

receiving a modulated signal representing symbols of information;

deriving quadrature component signals from the modulated signal;

generating a sample clock having a period equal to the period of a symbol clock for the modulated signal, the sample clock being shifted one-half period in phase with respect to the symbol clock;

sampling the quadrature component signals using the sample clock to produce pseudo-symbols as pairs of pseudo-symbols about a symbol sample point for each symbol; and

displaying the pseudo-symbols on a quadrature coordinate plane.

10. (Previously Presented) The method as recited in claim 9 further comprising the steps of:

generating a template representing locations of clusters of the pseudo-symbols for an ideal modulated signal, each cluster representing a symbol location; and

displaying the template on the quadrature coordinate plane.

11. (Original) The method as recited in claim 10 wherein the generating step comprises the step of calculating a diameter of a circle for each location, the template having the circle at each location representing the symbol location for the ideal modulated signal.

12. (Original) The method as recited in claim 11 wherein the calculating step comprises the steps of:

determining outer pseudo-symbol pairs for each symbol of the ideal modulated signal; and

calculating the diameter based on the outer pseudo-symbol pairs.

13. (Original) The method as recited in claim 10 further comprising the step of determining a quantitative index of distortion in the modulated signal as a function of the number of pseudo-symbols outside the template.

14. (Previously Presented) The method as recited in claim 9 wherein the displaying step comprises the step of zooming in on individual clusters of pseudo-symbols for the modulated signal to observe whether the arrangement of pseudo-symbols within the cluster is similar to the arrangement of the clusters on the quadrature coordinate plane.

Evidence Appendix

No evidence was submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132, and no other evidence was entered by the Examiner.

Related Proceedings Appendix

There are no related proceedings identified in this Brief.